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Low Power High Speed SAR ADCs Using Power Efficient Switchback Switching Method

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Abstract

This brief presents a low power , high speed successive approximation register analog to digital convertor that uses a power efficient switchback switching method and having high speed .With respect to other switching methods, in the switchback switching the input common mode voltage variation is reduced. Proposed switching method consumes less power and the SAR control logic module produce a high speed digital output which in turn produces an SAR ADC with high speed and power efficient.

Keywords- Energy *efficient switching method, SAR ADC.*

1.Introduction

With the feature size of CMOS device , propagation delay of the logic circuit decreases significantly .The successive approximation-register (SAR) analog-to-digital converters (ADCs) have achieved tens to Mega Sample per second to Low Giga sample per second sampling rates with 5 to 10 bit resolutions recently.

The comparator and sampling switches are the only analog components of successive approximation register analog to digital converters and no building block consumes static power if the preamplifiers are not used. Therefore , the Successive Approximation Register Analog –to- Digital converters are power and area efficient architecture.

In the past few years, several power- efficient switching sequences for the capacitive digital- to- analog converter (DAC) have been proposed. Compared to the other conventional switching sequence the energy saving monotonic and Vcm based switching sequence reduce about 69%, 81%, and 90% of switching energy respectively. Although the Vcm based one reduces the most power consumption the Vcm - based one reduces the most power consumption, it needs more switches and reference voltages than the monotonic one, which increase complexity and power consumption of the digital control circuits. The monotonic switching sequence has the fewest switches and reference voltages. However, during the conversion process, the common -mode voltage of the comparator input terminal varies from Vcm to Vrefn ,as shown in Fig. 1(a). It induces dynamic offset and the parasitic capacitance variation of the comparator to affect the ADC linearity. This brief mainly proposes a successive approximation ADC using switchback switching.

1.1 SAR ADC

With the feature size of CMOS devices scaled down, the prop-

Major components of this Successive Approximation Register Analog to digital converter include two sampling capacitors, two capacitive reference DACs, dynamic latched comparators and SAR Control logic. The proposed capacitive DAC is split into two parts which are the reference DAC and the sampling capacitor. The SAR control logic used here mainly consist of two D flip flops and two logic gates which are the EXOR gate and NAND gate. With the help of this circuit structure we can increase the speed of the whole successive approximation ADC.The power consumption is also reduced since the system uses a power efficient switchback switching procedure.

30-M

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525 μm .

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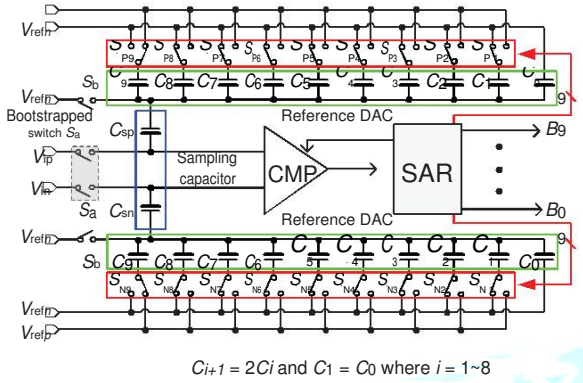

Fig. 2. Block diagram of the proposed ADC.

The SAR ADC has the fewest number of switches and reference voltages. Moreover the proposed switching sequence reduces 50% of the common mode voltage variation. Therefore, it can reduce the power consumption and design effort of the reference buffer.

The remainder of this brief is organized as follows. Section II describes the architecture and design concept of the proposed SAR ADC. Section III presents the implementation of key building blocks. Section IV shows the measurement results. Conclusions are given in Section V.

2. Architecture and Design concept of the Proposed SAR ADC

2.1 ADC Architecture

Fig. 2 shows the complete block diagram of the proposed ADC . The ADC core consists of two sampling capacitors, two capacitive reference DACs, dynamic-latched comparator and SAR control logic. The proposed capacitive DAC is split into two parts: a reference DAC and a sampling capacitor. The sampling capacitor captures the input signal and the reference DAC provides the reference signal. The reference DAC is a binary-weighted capacitor array which has better linearity than the C-2C capacitor array or the capacitor array with a bridged capacitor.

At the sampling phase, the switches S_a and S_b are turned on and the input signal is sampled onto the sampling capacitors, C_{sp} and C_{sn}. The bottom plate of the most-significant-bit (MSB) capacitor in the reference DAC is switched to $V_{ref\ p}$ and those of LSBs are switched to $V_{ref\ n}$ at the same time. Meanwhile, the reference DAC is at the reset state. Next, the switches S_a and S_b are turned off and the SAR ADC begins the conversion phase. The comparator determines whether V_{ip} is higher than V_{in} or not at the beginning of the conversion phase. If V_{ip} is higher than V_{in}, the MSB will be set to 1. Otherwise, the MSB is 0. Then the MSB triggers the SAR logic to control the reference switching of the DAC by the proposed switchback switching procedure.

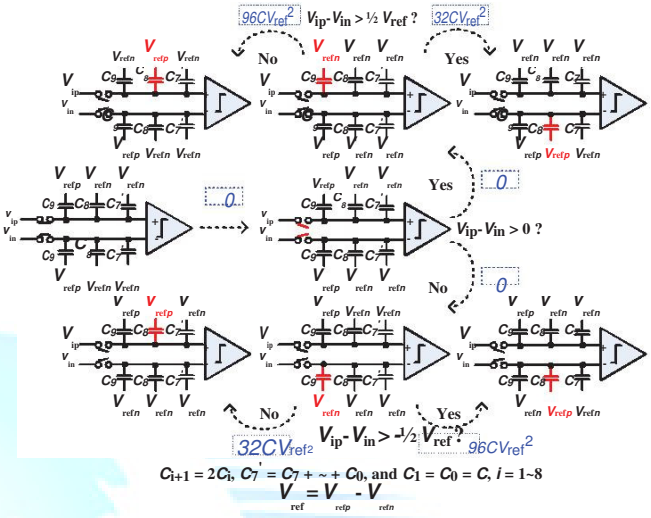

Fig. 3. Switchback switching procedure of 10-bit SAR ADC.

As the monotonic switching procedure, the switchback switching procedure only switches a capacitor in each bit cycle, which reduces both charge transfer in the capacitive DAC network and the transitions of the control circuit and switch buffer, resulting in smaller power dissipation. Moreover, the common-mode voltage of the switchback switching procedure would be downward just for the first switching and then upward for the remainder. Hence, the maximum variation of the common-mode voltage is 1/4 V_{ref} and the common-mode voltage will gradually approach the common-mode voltage of the input signal V_{cm}. It reduces the dynamic offset and the parasitic capacitance variation of the comparator.

Fig. 3 shows an example of the switchback switching method, where a 10-bit binary-weighted capacitive DAC is adopted and it is the same as the reference DAC adopted in Fig. 2. In order to simplify the illustration of the switchback switching method, the sampling capacitor of Fig. 2 is omitted in Fig. 3. The quantitative energy consumption of the first three switching phases is shown. For the switchback switching method, the bottom plate of the MSB capacitor is connected to $V_{ref\ p}$ and the rest are connected to V_{refn} at the sampling phase. Then the sampling switches turn off, the comparator directly performs the first comparison without switching any capacitor. After the MSB is determined, one MSB capacitor will switch to $V_{ref\ n}$. There is no energy consumption at this conversion step.

For a 10 bit case, the monotonic and Vcm based switching procedures consume 255.5 and 170.2 CVref square, respectively, while the proposed switching sequence consumes only 127.5 CVref square , which means the efficiency of the

proposed system is very high compared with that using the other switching procedures.

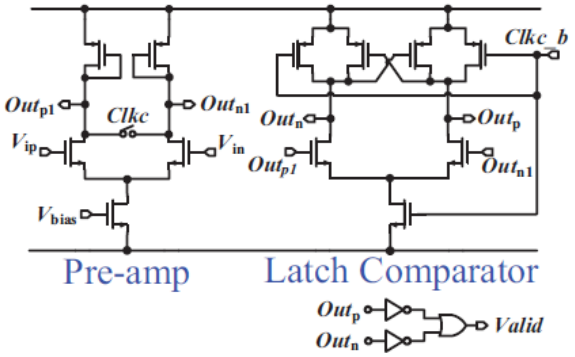

Fig. 4 The dynamic comparator with a pre-amplifier

The proposed switching procedure consumes only 127.5 CV^2_{ref} .The proposed technique thus requires 50% less switching energy than the monotonic one and 25% less than the V_{cm}-based one.

Although the switchback switching method consumes less power than the monotonic and V_{cm}-based switching methods during the conversion phase. It must be pre-charged in the sampling phase. For a 10-bit case, if all of the switching methods sample the same input signal, the switchback switching method consumes 255.5 CV^2_{ref} .

Accordingly, the switchback switching method may consume more power than the monotonic and V_{cm}-based switching methods if both sampling and conversion phases are taken into consideration. Nevertheless, it is worth to note that the switchback switching method reduces the design overhead of reference voltage circuit. The reason is for monotonic or V_{cm}-based switching methods, the MSB capacitor must settle to the reference voltage in a very short time during the conversion phase.

The MSB capacitor of switchback switching method is pre-charged in the sampling phase which allows longer settling time than the conversion phase. Therefore, the switchback switching method does not require a fast-settling reference buffer to charge MSB capacitor in the conversion phase.

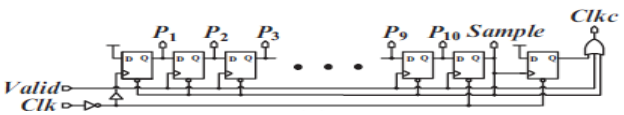

Fig.5 The SAR control logic

The D Flip flops present in the following circuit are replaced by an SAR cell which consist of two D flip flops and two logic gates. With the help of this SAR cell the overall speed of the proposed system increases and as a result performance also increases.

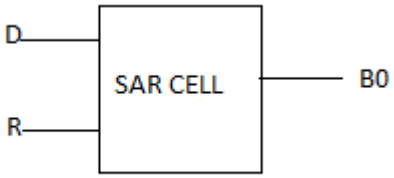

Fig. 6 The block of an SAR cell

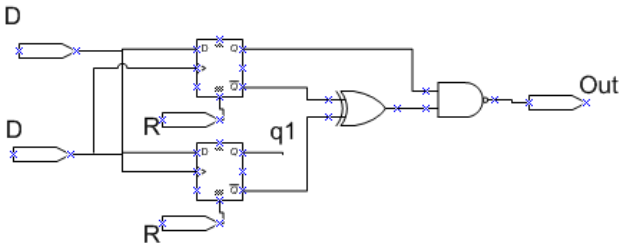

Fig.7 The circuit view of an SAR cell

The major working of this SAR cell is as follows. Mainly the SAR cell consist of two D flip flops in which both flip flops have common input. If one is given as input to both flip flops, the output Q will be one and Q bar will be zero. With two zeros as input to the XOR gives an output of zero. With 'Q' input and 'XOR output' as input to the NAND gate gives an output of one. In the same way if zero is given as input to both the flip flops also the final output fill be one.Thus this SAR cell helps to increase the speed of the proposed system.

3. Implementation of key building blocks

3.1 S/H circuit

The proposed SAR ADC samples input signal on the sampling capacitors, C_{sp} and C_{sn}, via the bootstrapped switches, S_a and S_b . The nonlinear variation of the parasitic capacitance during the conversion phase, induced by the sampling switch S_a and the comparator input pair, affects the linearity of the proposed SAR ADC. The top-plate parasitic capacitance of the sampling capacitor is a constant value, which does not affect the ADC performance. Sampling is the process of reduction of continuous signal to discrete form. At the same time sample is a value or set of value at a point in time or space. The common mode signal is a component of the analog signal which is the

average of the input signals. The input signals here are the Vdd and the ground signal which are being converted to digital signal. It is mainly used in high frequency applications and biomedical applications.

3.2 Dynamic Comparator

Fig.4 shows the schematic of the comparator which consists Of a pre-amplifier and a dynamic latched comparator. With a low sampling capacitance, the kickback noise originated from the latched comparator becomes more critical. Furthermore, the bottom plate of the sampling capacitors, C_{sp} and C_{sn}, are floating and hence sampling capacitors are more sensitive to kickback noise than the conventional case. Therefore, the proposed comparator adopts a pre-amplifier to block the kickback noise and enhance the comparison speed.

3.3 SAR Control Logic

To avoid a high-frequency clock generator and a pulse-width modulator (PWM), the proposed ADC uses an asynchronous control circuit to internally generate the necessary clock signals . Fig. 5 shows a schematic of an SAR control he conversion process starts once the system clock is switched to low. *Sample* is the sample signal which turns on the sampling switches. After ten comparisons, *Sample* will be set to high to sample the input signal until the system clock, *Clk*, switches to low. Therefore, the duty cycle of the system clock, *Clk*, is 50% and no PWM is needed for the integration application.

The dynamic comparator generates the *Valid* signal after each comparison. *Clkc* is the control signal of the dynamic comparator. P_1 to P_{10} sample the digital output codes of the comparator and serve as control signals for the capacitor arrays to perform the switchback switching procedure. With the proposed switching method, the minimum input capacitance decrease from 1025 to 328 fF. For routing parasitic capacitance, process variation and matching issues, the adopted values of C_{sp} and C are 400 and 5 fF, respectively. The sampling capacitors and reference DAC are metal-oxide-metal capacitors .

4. Measurement Results

The Analog to digital converter was fabricated in a 1P9M 90 –nm CMOS technology. The micrograph of the ADC is present. The ADC core occupies only an area of 525* 190 um. The ADC has a1.2 v peak – to – peak input range.The peak differential non linearity and integral non linearity are -0.66/0.88 and -1.27/1.32 LSB, respectively

At a 1.0V supply and 30 MS/s, the analog part including the S/H circuit and dynamic comparator, consumes 0.55 mW. The switching power of the reference DAC draws 0.08 mW and the digital control logic consumes 0.35 mW.

The pre-amplifier depletes most of the analog power (76%) because it consumes static power consumption.

The proposed switching sequence reduces the DAC switching power significantly; it just occupies 8.1% of the total power. Excluding the output buffers, the total power consumption is0.98 Mw. A specification summary of the analog to digital converter is listed in table I

To compare the proposed ADC to other works with different sampling rates and resolutions, the well-known figure-of-merit (FOM) equation is used

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \times \min\{2 \times \text{ERBW}, f_s\}}.$$

The FOM of the proposed ADC is 57 fJ/conversion-step at 30 MS/s and a 1.0-V supply. The pre-amplifier consumes 0.46 mW, which makes the FOM larger than the other works. Nevertheless, if the power consumption of the front-end buffer and reference buffer is considered, the FOM of the proposed ADC will be lower than the other works. Here the less area consuming Successive Approximation Register analog to digital converter is used which has an advantage of less delay. At the same time power efficient switchback switching algorithm is used for the system. Moreover this proposed system consist high speed SAR control logic module which provides a high speed operation without much delay. With the help of this the performance of the proposed system can be increased

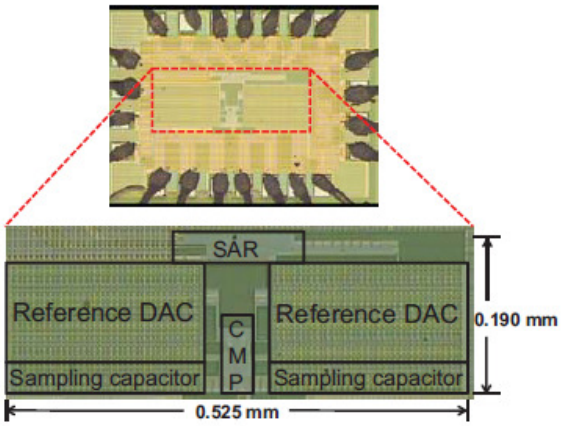

Fig 8. The die graph of the proposed system

The die micrograph of the ADC core is shown in the above figure which is a part of the proposed successive approximation register ADC system.

Specifications (unit)	Experimental results
Supply voltage (V)	1.0
Input range (V_{pp})	1.2
Active area (mm^2)	0.10
Input capacitance (pF)	0.4
Sampling rate (MS/s)	30
DNL (LSB)	$-0.66 \sim 0.88$
INL (LSB)	$-1.27 \sim 1.32$
ENOB (bit)	9.16 @ 30 MS/s
SNDR/SFDR (dB)	56.89/68.65 (0.5 MHz)
	56.25/68.15 (2 MHz)
ERBW (MHz)	15 @ 30 MS/s
Power (mW)	0.98
FOM (fJ/conv.-step)	57

Table I.The specification and results of the proposed system

5. Conclution

In this brief, a successive approximation register analog to digital converter with a new switching method and a modified SAR control logic which provide high speed and low power consumption is presented. The proposed SAR control logic mainly consist of flip flop and logic gates which helps in the speed enhancement. The proposed switching procedure reduces the parasitic capacitance variation and the comparator dynamic offset induced by input common mode voltage variation. The input capacitance of the proposed successive approximation register analog to digital converter is just 0.4 pf which reduces the power consumption and design effort of the front end buffer. The prototype mainly occupies an active area of 0.1mm square and achieves more than 30 Ms/s operation speed with a power consumption less than 1 Mw.

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Chinju Skariah received the B. Tech Degree in Electronics and Communication (ECE) Engineering from MBC College of Engineering and Technology, India in 2012. She is currently pursuing the Masters Degree from PPG Institute of Technology, Coimbatore , Anna University, Chennai. Her current research interest include low power, high speed, high performance and robust circuit design for SAR ADC using deep submicron CMOS technology.

Anna George received the B. Tech Degree in Electronics and Communication (ECE) Engineering from Ilahia College of Engineering and Technology, India in 2012. She is currently pursuing the Masters Degree from PPG Institute of Technology, Coimbatore , Anna University, Chennai. Her current research interest include low power, high performance and robust circuit design for self healing VCO using pre-scalar for PLL.

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